International Journal of Electronics Communication and Computer Engineering
Volume 4, Issue 1, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

Design, Implementation and Performance Analysis of 4-bit Full Ripple Carry Adder Using Adibatic Logic in 45nm CMOS Sub-micron Technology

Jitendra R. Patel, Prof. Sandip Nemade, Prof. Vikas Gupta

Abstract — **In this paper I had implemented the different three types of 4-bit adder using adiabatic logic and conventional CMOS logic in 45nm technology with LT spice. As we know Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc. we have compared all three techniques conventional CMOS, 1n-1p Quasi and 1n-1p split level logic in 1-bit as well as 4-bit adder for power dissipation and as result suggest adiabatic method has low power dissipation compared to conventional CMOS. We got minimum power dissipation and energy consumption in 1n-1p split adiabatic logic.**

Keywords — **Adibatic Logic, DSP, CMOS, Low Power.**

I. Introduction

Power consumption and it's minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation and it can lead to reliability and IC packaging problems.

Adiabatic logic reduces the energy dissipation by reducing the dissipation across resistances of conducting MOSFETs and recovering the part of energy given to the output back to the source, which extends the battery life. Several adiabatic logic styles are available but here we implemented two styles are 1n-1p Quasi adiabatic logic and 1n-1n Split level adiabatic logic. As we know Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc.

II. Adiabatic and Conventional Charging

A. Conventional charging

The dominant factor of power dissipation in a conventional CMOS device is the dynamic power required to charge and discharge the capacitive nodes within the circuit itself. To charge the node capacitance CL from a dc supply of potential VDD, an energy

$$E = C_L . V_{DD}^2 \qquad (1)$$

Is withdrawn from supply. Only half of this energy is temporarily stored in capacitor CL. The remaining

$$E = 0.5 C_L . V_{DD}^2 \qquad (2)$$

Is dissipated as heat in the on resistance of PMOS. When input becomes logic high, the NMOS turns on and energy stored on capacitor CL is discharged to the ground and dissipated as heat. Hence during a complete charge-discharge cycle, the energy

$$E = C_L . V_{DD}^2 \qquad (3)$$

Is withdrawn from power supply and is dissipated as heat. Half of this energy is dissipated during charging and half is dissipated during discharging.

B. Adiabatic Charging

When you submit your final version, after your paper has been accepted, prepare it in two-column format, including figures and tables.

In static CMOS logic, the abrupt application of supply voltage gives rise to high potential across the switching device. The energy dissipation during charging and discharging can be minimized to a great effect by ensuring that the potential across switching device is kept sufficiently small. Adiabatic charging may be achieved by charging the capacitor from a time varying source that starts at 0V. This time varying source rises towards V at a slow rate that ensures that potential across switching device is kept arbitrarily small. The adiabatic charging is shown in figure 1.

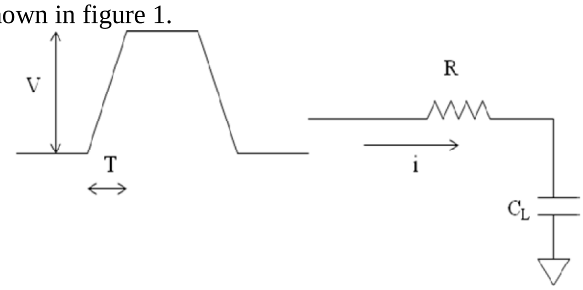

Fig.1. Adiabatic charging

In fact the energy dissipated across the resistance, R is

$$E_{diss.} = I^2 . RT = \frac{RC}{T} . C . V_{DD}^2 \qquad (4)$$

From the above equation (4), we can see that if T >> RC, the energy dissipation during charging Ediss ≈ 0. Same is applicable during discharge process. In addition to this, in some adiabatic logics, the energy dissipation also occurs due to threshold voltage of MOSFET and diode cut-in voltage. The energy dissipation due to threshold voltage Vt is

$$E = 0.5 C V_t^2 \qquad (5)$$

The energy dissipation due to diode cut-in voltage Vd is

$$E = C_L V_d V_s \qquad (6)$$

International Journal of Electronics Communication and Computer Engineering
Volume 4, Issue 1, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

Where, Vs is the voltage swing.

III. Design and Implementation of Adders

Different adiabatic logic styles contain different number of transistors and different number of power clocks. In this section we will study different adiabatic logic styles, which are derived from static CMOS, without large change: 1n1p split-level pulse adiabatic logic, 1n1p quasi adiabatic logic and conventional CMOS style from which both adiabatic style are derived.

A. 1n-1p Quasi full adder

The 1n1p quasi adiabatic logic basically, it is similar to conventional CMOS except, it includes a sinusoidal power clock instead of dc power supply. By implementing 1n1p quasi adiabatic logic, it is possible to achieve quasi adiabatic operations with conventional static CMOS gates under one phase driving. If driver is varied sufficiently slowly, dissipation occurs only during charging and discharging of load capacitor [7]. The sources of power dissipation in 1N1P quasi adiabatic logic are threshold voltage of MOSFET and energy dissipated in NMOS and PMOS resistance while charging and discharging of load capacitance. The use of slowly varying power clocks ensures the small energy dissipation across the ON resistance of MOS devices.

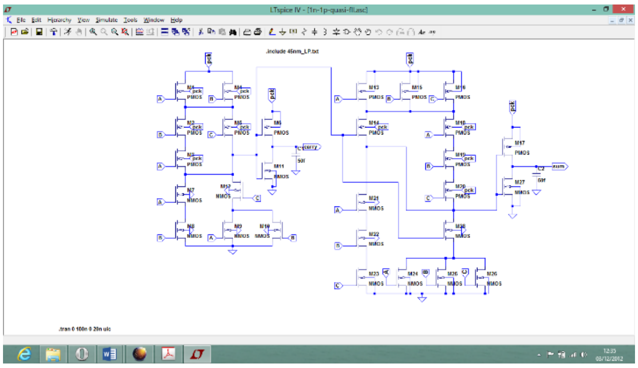

Fig.2. Schematic of 1-bit 1n-1p quasi full adder

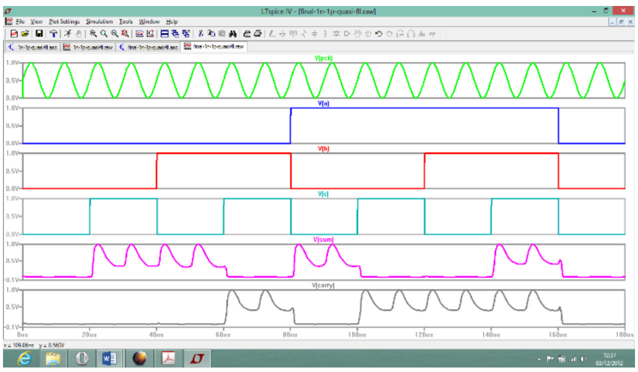

Fig.3. Simulation result of 1-bit 1n-1p quasi full adder

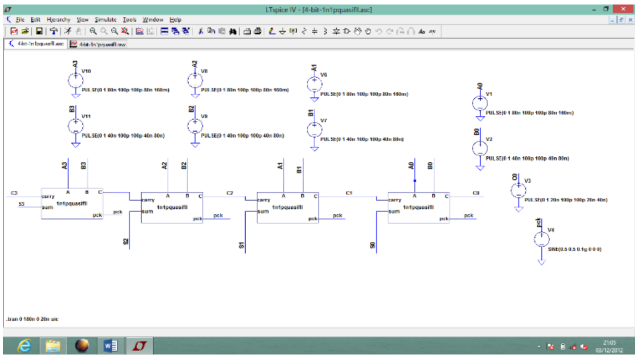

Fig. 4 Schematic of 4-bit 1n-1p quasi ripple carry full adder

Figure 2, and figure 3 shows schematic of 1-bit full adder and it’s simulation result, while figure 4, and figure 5 shows 4-bit ripple carry adder and it’s simulation result.

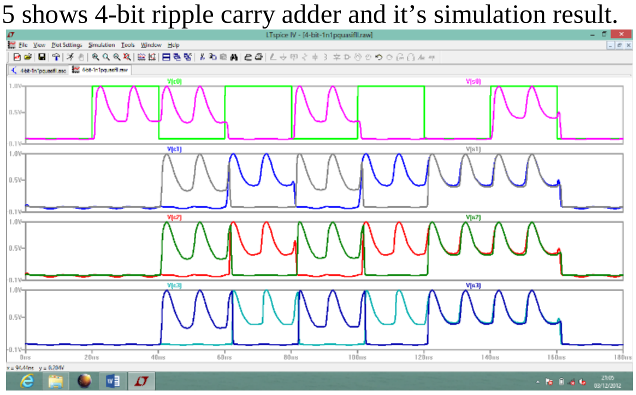

Fig.5. Simulation result of 4-bit 1n-1p quasi ripple carry full adder

B. 1n-1p Split level adder

The second adiabatic logic family that we are going to discuss is 1n1p split-level pulse adiabatic logic. It comprises a conventional CMOS gate with two complimentary split-level pulse voltages. The peak voltage of each clock supplies is VDD/2 to the gates. In this logic family, the dissipation occurs solely from a finite rate of change of driving voltage and can be decreased to any desired level figure 6, and figure7 shows the schematic and its simulation result for 1 bit full adder, while figure 8, and figure 9 shows 4-bit ripple carry full adder.

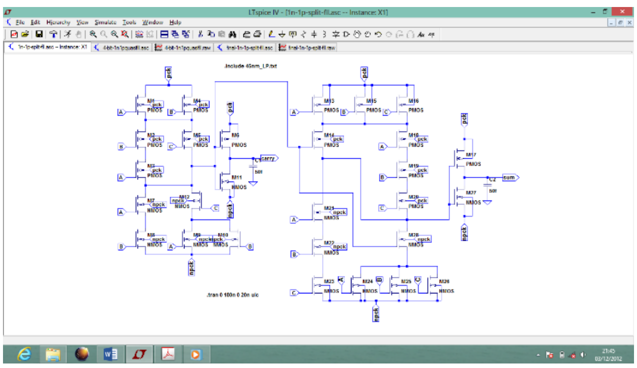

Fig.6. Schematic of 1-bit 1n-1p split full adder

International Journal of Electronics Communication and Computer Engineering
Volume 4, Issue 1, ISSN (Online): 2249–071X, ISSN (Print): 2278–4209

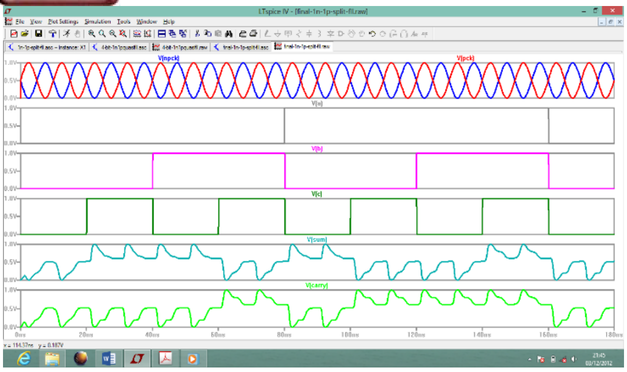

Fig.7. Simulation result of 1-bit 1n-1p split full adder

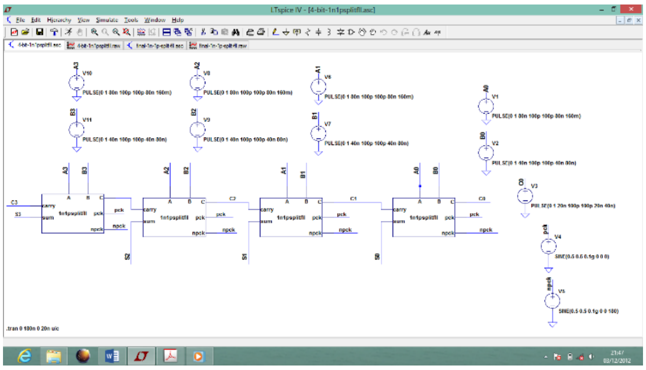

Fig.8. Schematic of 4-bit 1n-1p split ripple carry full adder

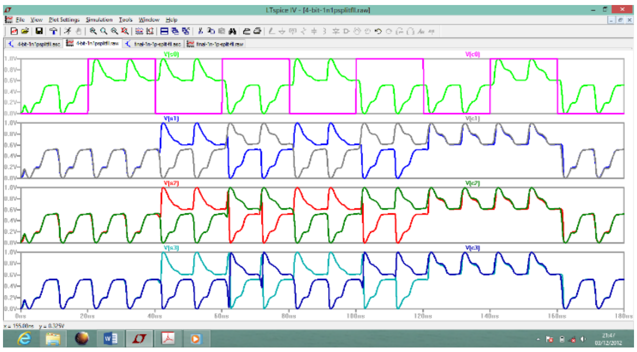

Fig.9. Simulation result of 4-bit 1n-1p split ripple carry full adder

C. *Conventional adder*

The conventional full adder design using static CMOS design the schematics to realize the Carry and Sum functions of a full adder are shown in figure 10, figure 11 shows it's simulation result, while figure 12, figure 13 shows 4-bit ripple carry adder and simulation result of it.

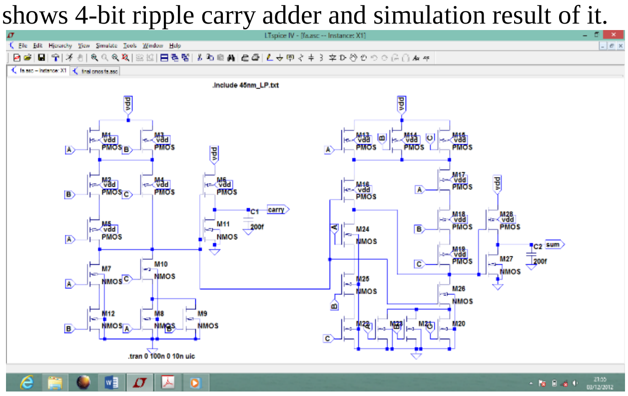

Fig.10. Schematic of 1-bit static CMOS full adder

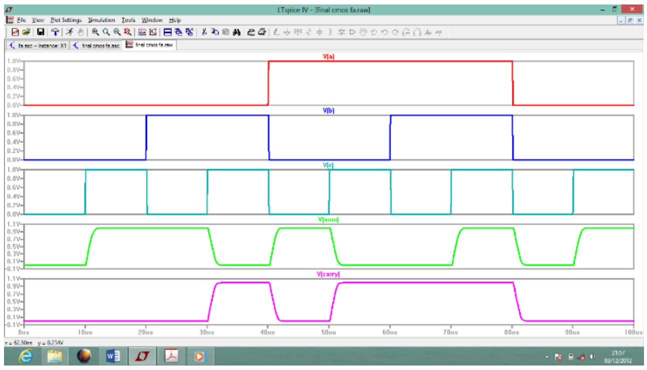

Fig.11. Simulation result of 1-bit static CMOS full adder

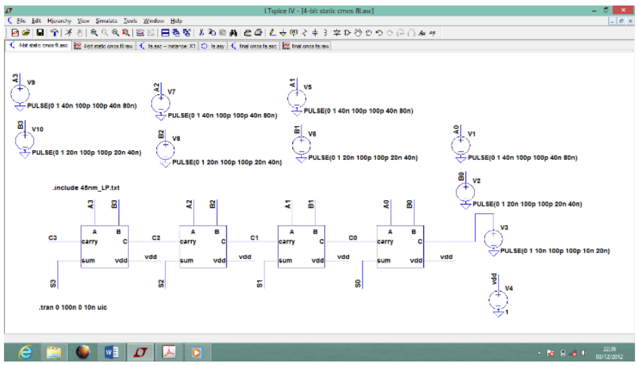

Fig.12. Schematic of 4-bit static CMOS ripple carry full adder

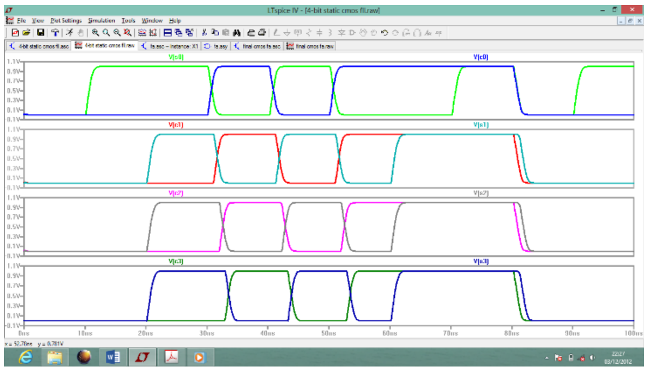

Fig.13. Simulation result of 4-bit static CMOS ripple carry full adder

IV. Comparative Analysis of Adders

As we analysis all three adder in 1-bit as well as 4-bit adder by varying the load capacitance start from 10fF to 200fF, by applying power clock of 100MHz, other inputs of 6.25MHz, 12.5MHz and 25MHz respectively.we are increasing load capacitance dissipated power also increasing. By comparative analysis we can see that adiabatic logic has low dissipation power compared to static CMOS logic and from two adiabatic logic 1n-1p Quasi has a least power dissipation at 1v power clock. Table 1 and table 2 shows the average power consumption for 1-bit and 4-bit adder respectively.

Table 1: Power Dissipation of 1-bit Full Adder

Load Capacitance (fF)	Average Power Dissipation (uW)		
	Static CMOS	1n-1p Quasi	1n-1p Split
10	2.125	0.4169	0.3194
20	2.73	0.6471	0.5376
30	3.35	1.5433	0.759
40	3.646	1.8135	0.9512
50	4.5534	2.0918	1.2555
60	4.6666	2.3643	1.6109
70	4.8707	2.6743	1.9631
80	5.5003	2.9662	2.1406
90	6.4513	3.2789	2.3215
100	6.6942	3.6096	2.6773
110	7.8996	3.9331	3.1339
120	8.1746	4.2426	3.4604
130	9.381	4.5822	3.6815
140	9.7949	4.9478	3.9211
150	9.9574	5.2883	4.4426
160	11.193	5.6575	4.7299
170	11.84	5.9887	5.0778
180	11.892	6.3642	5.2832
190	12.405	6.6755	5.5597
200	12.947	7.0488	6.0898

Table 2 : Power Dissipation of 4-bit Adiabatic Full Adder

Load Capacitance (fF)	Average Power Dissipation (uW)	
	1n-1p Quasi	1n-1p Split
10	0.4361	0.4761
20	0.9357	0.8084
30	1.4128	1.1459
40	2.296	1.6456
50	2.7217	2.0002
60	2.9404	2.4141
70	3.128	2.8419
80	3.3924	3.195
90	3.7685	3.387
100	4.7619	3.7564
110	5.1394	3.9368
120	5.5159	4.2973
130	5.8369	4.5781
140	6.1258	4.6773
150	6.4168	5.0115
160	6.6918	5.0544
170	7.0066	5.6709
180	7.3269	6.2391
190	7.6384	6.7017
200	7.8281	7.2041

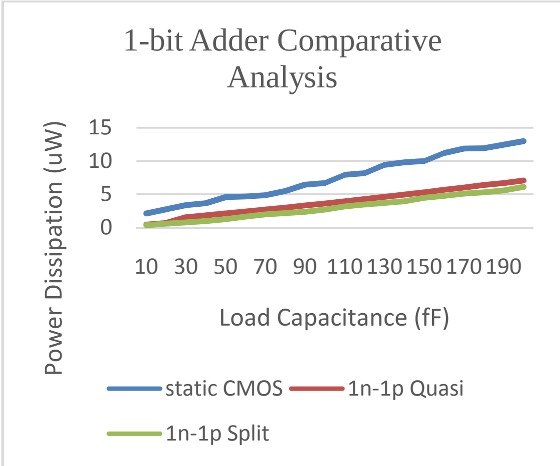

Fig.14. Graphical representation of 1-bit adder power dissipation

V. Conclusion

From all results display by graph and observed from the table 1 and table 2, we comes to know the adiabatic family has a low power dissipation compared to static CMOS adder, while in adiabatic technology 1n-1p Quasi has the high power dissipation as shown in graphical representation the power dissipation is linearly increases with increase in load capacitance, whereas in 1n-1p split level somewhat lower power dissipation

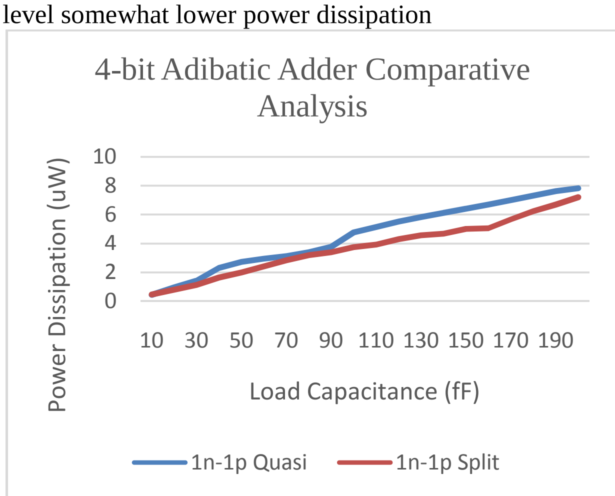

Fig.15. Graphical representation of 4-bit Adibatic adder power dissipation

Acknowledgment

I want to sincerely say thanks to my guide Proff. Sandip Nemae to guide and choose such a level of work for me, at last but not least I thank full to all staff of department who help me directly or indirectly.

References

[1] Praveen Saxena, dinesh Chandra and Sampath kumar, *Design Of "A 1-Bit Full Adder For Low Power Application"*, in (IJAEST) International Journal Of Advanced Engineering Sciences And Technologies Vol No. 10, Issue No. 1, 019 – 025, 2011.

[2] Y. Sunil Gavaskar Reddy and V.V.G.S.Rajendra Prasad, *"The Power Comparison Of Cmos And Adiabatic Full Adder Circuits"* in International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.3, September 2011.

[3] Praveen Saxena, dinesh Chandra and Sampath kumar, *"An Adiabatic Approach For Low Power Full Adder Design"*, in International Journal on Computer Science and Engineering (IJCSE) Vol. 3 No. 9 september 2011.

[4] Subodh Wairya, Rajendra Kumar Nagaria and Sudarshan Tiwari, *"Comparative Performance Analysis of XOR/XNOR Function Based High-Speed CMOS Full Adder Circuits For Low Voltage VLSI Design,"* in International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.2, April 2012.

[5] A. Kishore Kumar, D. Somasundareswari, V. Duraisamy, T. Shunbaga Pradeepa, *"Design of Low Power Full Adder using Asynchronous Adiabatic Logic"* in European Journal of Scientific Research ISSN 1450-216X Vol.63 No.3 (2011), pp. 358-367.

[6] The Manoj Kumar, Sandeep K. Arya and Sujata Pandey, *"Single bit full adder design using 8 transistors with novel 3 transistors XNOR gate"* in International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.4, December 2011.

[7] R.UMA, Vidya Vijayan, M. Mohanapriya, Sharon Paul, *"Area, Delay and Power Comparison of Adder Topologies"* in International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012.

[8] Jin-Fa Lin, Yin-Tsung Hwang, Ming-Hwa Sheu, and Cheng-Che Ho, *"A Novel High-Speed and Energy Efficient 10-Transistor Full Adder Design"* IEEE Trans. Circuits and Systems, vol. 54, No. 5, pp. 1050–1059, May 2007.

[9] Dai Jing. Hu Jianping, Zhang Weiqiang, Wang Ling, *"Adiabatic CPL circuits for sequential logic systems"*, IEEE MWSCAS'06, pp.713-717, August 2006.

[10] Ilham Hassoune and Denis Flandre, *"ULPFA: A New Efficient Design of a Power-Aware Full Adder"* IEEE Trans. Circuits and Systems, vol. 57, No. 8, pp. 2066–2074, August 2010.

[11] Jianping Hu; Weiqiang Zhang; Xien Ye; Yinshui Xia; *"Low power adiabatic logic circuits with feedback structure using three-phase power supply"*, in Proceedings of International Conference on Communications, Circuits and Systems, Vol. 2, 27-30, May 2005.

[12] A. P. Chandrakasan, S. Sheng and R. W. Bordersen, (1992) *"Low-power CMOS digital design,"*IEEE Journal of Solid-State Circuits, Vol. 27, No. 4, pp. 473- 484.

[13] Abdulkarim Al-Sheraidah, Yingtao Jiang, Yuke Wang and Edwin Sha, (2001) *"A Novel Low Power Multiplexer-Based Full Adder,"* European Conference on Circuit Theory and Design, Espoo, Finland, pp. I329-I332.

[14] Uming Ko, Poras T. Balsara and Wai Lee, (1995) *"Low-Power Design Techniques for High- Performance CMOS adders,"* IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 3, No. 2, pp. 327-333.

[15] Subodh Wairya , Garima Singh, Vishant, R. K. Nagaria and S. Tiwari (2011), *"Design Analysis of XOR (4T) based Low Voltage CMOS Full Adder Cell,"* In Proceeding of IEEE International Conference on Current Trends In Technology (NUiCONE'11), Ahmedabad, India pp. 1-7.

AUTHOR'S PROFILE

Jitendra R. Patel

A post graduate student of Technochrate Institute of Technology, Bhopal, RGPV university, MP, India. Has graduation in Electronics and Communication from shri C.U.Shah college of Engg. And technology, Wadhwan city, Saurastra university, Rajkot, Gujrat, India. My area of interest is VLSI design and it's methodologies, Wireless communication and microelectronics.